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The cost to testing the associated IPs is also on the rise. To mitigate this post silicon validation and debug challenge, design teams have resorted in applying on-chip debug strategy, more automated techniques for post-silicon test generation and pre-tapeout assertions for effective coverage/analysis.

### **Accelerating Post-Silicon Debug and Test - SemiWiki**

Turning on GPU-based validation GBV can be forced on using the DirectX Control Panel (DXCPL) by forcing on the Direct3D 12 Debug Layer and additionally forcing on GPU-based validation (new tab in the control panel). Once enabled, GBV will remain enabled until the Direct3D 12 device is released.

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Session: Accelerating SOC Debug and Validation at Quality. ... In this presentation, we will share how these data availability problems affect test creation, test execution and failure debug. We ...

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